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FDG6318P

Dual P-Channel, Digital FET

General Description

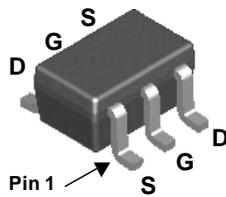
These dual P-Channel logic level enhancement mode MOSFET are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETS.

Applications

- Battery management

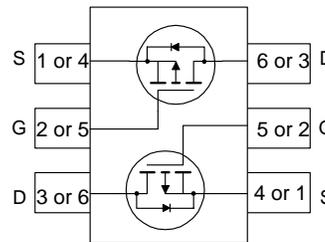
Features

- -0.5 A, -20 V. $R_{DS(ON)} = 780\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 1200\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- Very low level gate drive requirements allowing direct operation in 3V circuits ($V_{GS(th)} < 1.5\text{ V}$).
- Compact industry standard SC70-6 surface mount package



SC70-6

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|------------------|
| V_{DSS} | Drain-Source Voltage | -20 | V |
| V_{GSS} | Gate-Source Voltage | ± 12 | V |
| I_D | Drain Current – Continuous (Note 1) | -0.5 | A |
| | – Pulsed | -1.8 | |
| P_D | Power Dissipation for Single Operation (Note 1) | 0.3 | W |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Thermal Characteristics

| | | | |
|-----------------|--|-----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 415 | $^\circ\text{C/W}$ |
|-----------------|--|-----|--------------------|

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|----------|-----------|------------|------------|
| .38 | FDG6318P | 7" | 8mm | 3000 units |

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|--|-----|-----|-----------|----------------------|
| BV_{DSS} | Drain–Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | -10 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| I_{GSS} | Gate–Body Leakage | $V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 100 | nA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|--|-------|-------------------|-------------|----------------------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -0.65 | -1.2 | -1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | 2 | | mV/ $^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -0.4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}, T_J = 125^\circ\text{C}$ | | 580 980 780 | 780 1200 | m Ω |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$ | -1.8 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = -5\text{ V}, I_D = -0.5\text{ A}$ | | 1.1 | | S |

Dynamic Characteristics

| | | | | | | |
|------------|------------------------------|---|--|------|--|----------|
| C_{iss} | Input Capacitance | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 83 | | pF |
| C_{oss} | Output Capacitance | | | 20 | | pF |
| C_{riss} | Reverse Transfer Capacitance | | | 11 | | pF |
| R_G | Gate Resistance | $V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$ | | 12.1 | | Ω |

Switching Characteristics (Note 2)

| | | | | | | |
|--------------|---------------------|---|--|------|-----|----|
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD} = -10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$ | | 6 | 12 | ns |
| t_r | Turn–On Rise Time | | | 12 | 22 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 6 | 13 | ns |
| t_f | Turn–Off Fall Time | | | 1 | 3 | ns |
| Q_g | Total Gate Charge | $V_{DS} = -10\text{ V}, I_D = -0.6\text{ A},$ $V_{GS} = -4.5\text{ V}$ | | 0.86 | 1.2 | nC |
| Q_{gs} | Gate–Source Charge | | | 0.22 | | nC |
| Q_{gd} | Gate–Drain Charge | | | 0.25 | | nC |

Drain–Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|--|--|-------|-------|----|
| I_S | Maximum Continuous Drain–Source Diode Forward Current | | | | -0.25 | A |
| V_{SD} | Drain–Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = -0.25\text{ A}$ (Note 2) | | -0.83 | -1.2 | V |
| t_{rr} | Reverse Recovery Time | $I_F = -0.5\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$ | | 12.6 | | ns |
| Q_{rr} | Reverse Recovery Charge | | | 2.52 | | nC |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA} = 415^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

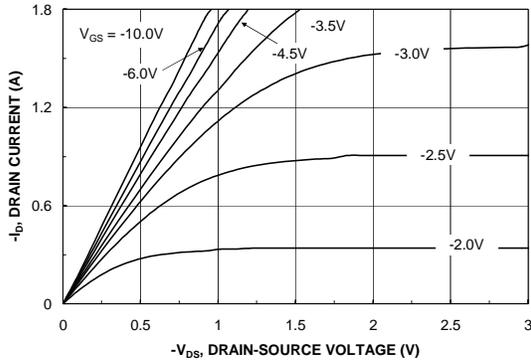


Figure 1. On-Region Characteristics.

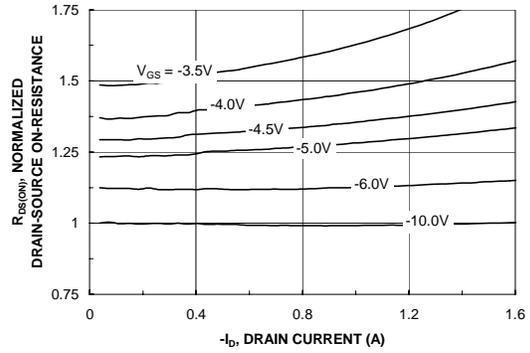


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

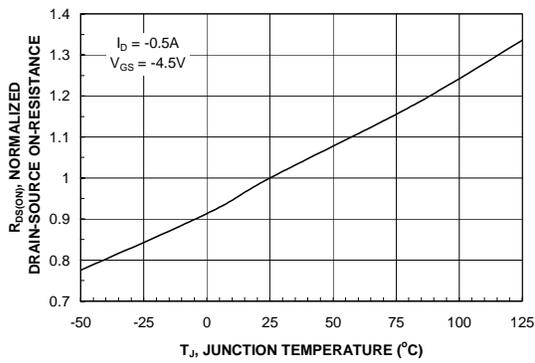


Figure 3. On-Resistance Variation with Temperature.

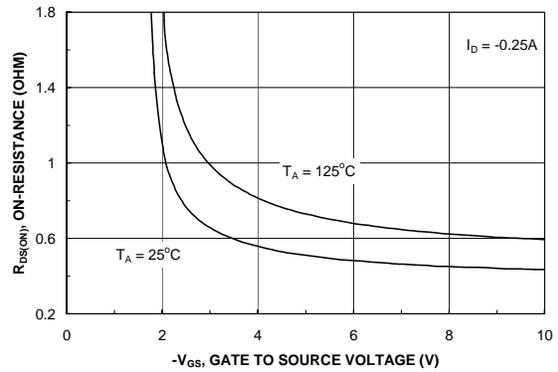


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

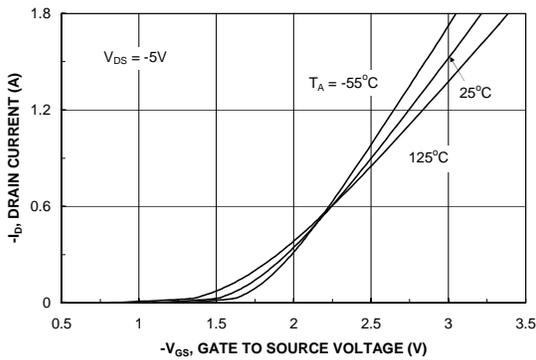


Figure 5. Transfer Characteristics.

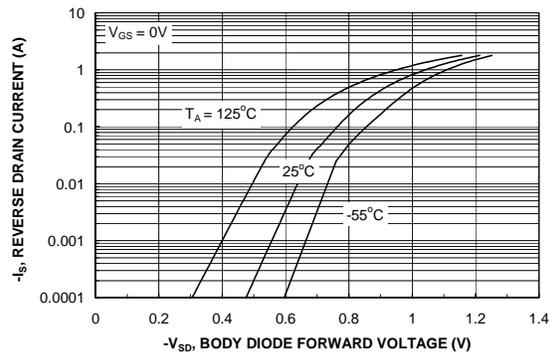


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

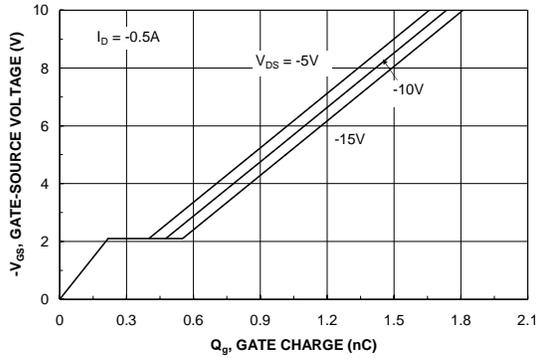


Figure 7. Gate Charge Characteristics.

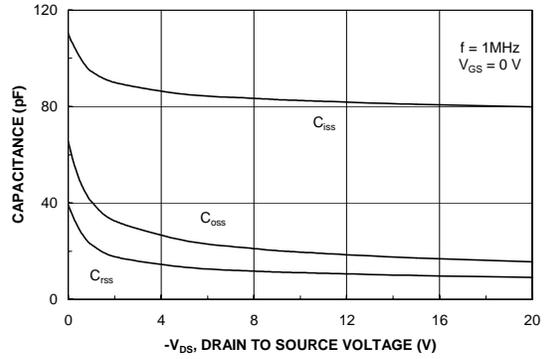


Figure 8. Capacitance Characteristics.

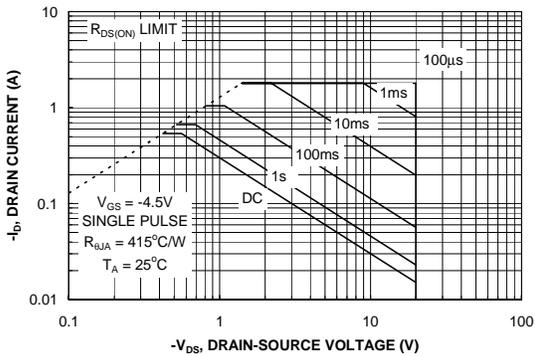


Figure 9. Maximum Safe Operating Area.

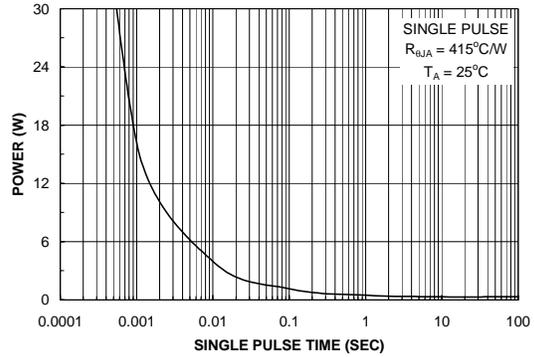


Figure 10. Single Pulse Maximum Power Dissipation.

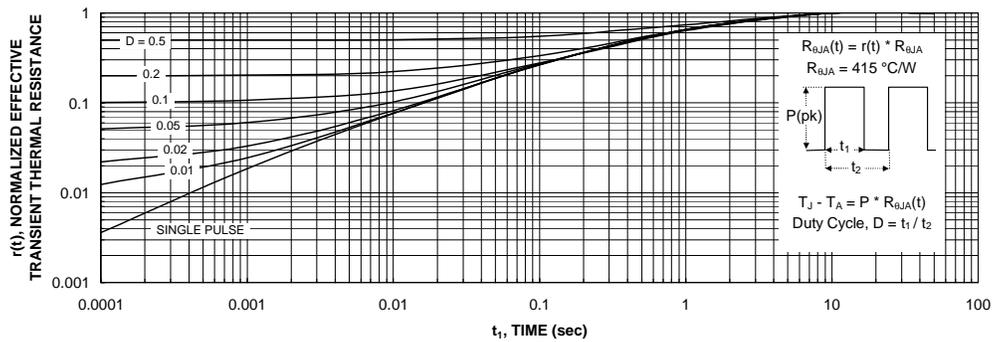


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

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